IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PROMOS TECHNOLOGIES, INC.,	)	
	)	
Plaintiff,	)	
	)	
v.	)	C.A. No. 06-788 (JJF)
	)	
FREESCALE SEMICONDUCTOR, INC.,	)	
	)	
Defendant.	)	

REVISED TAB 1B TO FREESCALE'S OPENING CLAIM CONSTRUCTION BRIEF

Attached is a revised version of Tab 1B to Freescale's Opening Claim Construction Brief (D.I. 85).

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REVISED TAB 1B
(TO FREESCALE'S OPENING CLAIM CONSTRUCTION BRIEF, D.I. 85)

ProMOS Technologies, Inc. v. Freescale Semiconductor, Inc., (D. Del.) CA No. 06-788 (JJF)

12-13-2007

Parties' Proposed Claim Constructions for the Chan '709 and '241 Patents

Chan Claim Limitation	Freescale's Constructions	ProMOS's Constructions
cache memory apparatus*	A memory chip that is external to the CPU chip.	Does not need construction.
cache memory*	Does not need to be construed because it is not a claim term.	Small block of high speed memory associated with a computer processor/ microprocessor (CPU).
host port*	A set of pins on the cache memory chip used for the input and output of data over the host data bus. **Alternative:** [A set of pins] Point of access structure on the cache memory chip package used for the input and output of data over the host data bus.	Interface between a cache memory and a host processor or host data bus.
system port*	A set of pins on the cache memory chip used for the input and output of data over the system data bus. **Alternative:** [A set of pins] Point of access structure on the cache memory chip package used for the input and output of data over the system data bus.	Interface between a cache memory and a system memory or system data bus.
dual port cache memory*	~~A cache memory chip having a host port and a system port.~~ A memory chip that is external to the CPU chip.	A cache memory that has two interfaces.
cache controller	A chip that controls a cache chip.	Circuitry that controls the transfer of data or other information to and from cache memory.
controller	A chip that controls a cache chip.	Does not need construction.

Chan Claim Limitation	Freescale's Constructions	ProMOS's Constructions
first port*	Set of pins on cache controller chip used for the input and output of address information over the host address bus. **Alternative:** [Set of Pins] Point of access structure on cache controller chip package used for the input and output of address information over the host address bus.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a port connected to the host address bus.
second port*	Set of pins on cache controller chip used for the input and output of address information over the system address bus. **Alternative:** [Set of pins] Point of access structure on cache controller chip package used for the input and output of address information over the system address bus.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a port connected to the system address bus.
host	A single chip central processing unit (CPU)	~~CPU associated with one or more cache memories.~~ Does not need construction.
host microprocessor	A single chip central processing unit (CPU).	CPU associated with one or more cache memories.
host processor	A single chip central processing unit (CPU).	CPU associated with one or more cache memories.
bus*	Does not need to be construed because it is not a claim term but means: a set of conductors used to transfer data between devices.	Line or set of lines used to transfer data or other information.
host address bus	A set of conductors connected to the address terminal pins of a CPU chip used to transfer memory addresses from the CPU to other components of a computer system.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a bus for providing a host address.
host data bus	A set of conductors connected to the data terminal pins of the CPU used to transfer data to and from the CPU and other components of a computer system.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a bus for providing a host address.

Chan Claim Limitation	Freescale's Constructions	ProMOS's Constructions
buffering	Using a storage element (e.g., memory write register) as an intermediary device to hold data temporarily while the data is waiting to be transferred from one external device (e.g., the CPU) to another external device (e.g., system memory) because of differences in rates of data flow or time of occurrence of events.	Storing data temporarily to compensate for differences in rates of data flow, time of occurrence of events, or amounts of data that can be handled by the devices or processes involved in the transfer or use of data.
means for identifying ones of the fetched data held in said memory update register as not corresponding to ones of the second data held in said write back register for write back to said system port	Indefinite – no corresponding structure disclosed in the specification.	Means plus function. Function: identifying ones of the fetched data held in said memory update register as not corresponding to ones of the write back data held in said write back. register for write back to said system port. Corresponding Structure: the valid bits associated with the memory update register set 116.
means for identifying ones of the fetched data held in said memory update register as not corresponding to ones of the write back data held in said write back register for write back to said system port	Indefinite – no corresponding structure disclosed in the specification.	Means plus function. Function: identifying ones of the fetched data held in said memory update register as not corresponding to ones of the write back data held in said write back register for write back to said system port. Corresponding Structure: the valid bits associated with the memory update register set 116.
means for masking the providing of selected ones of said words of the fetched data to said random access memory	Indefinite – no corresponding structure disclosed in the specification.	Means plus function. Function: masking the providing of selected ones of said words of the fetched data to said random access memory. Corresponding Structure: the mask bits associated with the memory update register set 116.

Chan Claim Limitation	Freescale's Constructions	ProMOS's Constructions
means for masking writing of selected words of data into said random access memory	Indefinite – no corresponding structure disclosed in the specification.	Means plus function. Function: masking writing of selected words of data into said random access memory. Corresponding Structure: the mask bits associated with the memory update register set 116.
means for disabling said dual port cache memory during a local bus access cycle	Indefinite – no corresponding structure disclosed in the specification.	Means plus function. Function: disabling said dual port cache memory during a local bus access cycle. Corresponding Structure: circuitry within the Controller 70 that evaluates host address and control signals and determines when a host bus cycle is not passed on to the system bus and does not cause a cache hit/miss determination. This includes the circuitry within Local Processor Interface Unit 220 and Control Register Interface Unit 224. Operation of the circuitry is described at 42:58-43:42, with reference to Fig. 37 and 38 and in Table VI at 39:27-35.
first control sequencer for controlling addressing and data signals on said host address bus and on said host data bus	Indefinite – no corresponding structure disclosed in the specification.	Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent that Freescale is suggesting that the term “first control sequencer” needs to be construed, and to the extent the Court decides to construe the term, it means: a first machine which puts items of information into a particular order. (Not means plus function).
operations at said system port to be decoupled from said random access memory	Indefinite.	
operably decoupled	Indefinite.	Does not need construction.

Chan Claim Limitation	Freescale's Constructions	ProMOS's Constructions
register*	Does not need to be construed because it is not a claim term but means: a set of bits of high-speed memory within an electronic device, used to hold data for a particular purpose.	Circuitry capable of retaining data or other information, such as address information
host input register	Indefinite.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: (in claim 10) a register connected to the host port (in claim 15) a register coupled to the addressable memory storage and the host data bus.
system input register	Indefinite.	Does not need construction.
system output register	Indefinite.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a register connected to the system port.
first input register	Indefinite.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a register for selectively writing input data to the addressable storage.
first output register	Indefinite.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a register for selectively furnishing output data to the system port.
second input register	Indefinite.	Does not need construction; meaning is clear from the claim language. To the extent the Court decides to construe the term, it means: a register for providing second input data to the addressable storage.

Chan Claim Limitation	Freescale's Constructions	ProMOS's Constructions
~~a data path between said host data bus and said system data bus is operably decoupled by~~ buffering and selective provision of data to and from said cache storage locations by said plurality of registers* ~~so as to allow concurrent transfer of data to and from said dual port cache memory~~	The claim phrase "~~operably decoupled by~~ buffering and selective provision of data to and from said cache storage locations by said plurality of registers" is indefinite.	Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. See ProMOS's position on "operably decoupled", "buffering," "selective provision", "plurality of registers" and "to allow", above. The term "data path" is clear on its face and does not require construction.
system memory	Main memory of a computer system that is external to the CPU chip	Main memory of a computer, relatively larger and slower than cache memory.
first input data being provided to said random access memory from said memory write register at the same time that the first output data is provided by said write back register to said system port	Whenever the first input data is provided to the RAM, the first output data must be provided to the system port.	Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent Freescale is suggesting that the terms "being provided" and "at the same time" need to be construed, these terms are clear on their face.
wherein the input data is provided to said random access memory from said memory write register at the same time that the output data is provided by said write back register to said system port	Whenever input data is provided to the RAM, output data must be provided to the system port.	Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent Freescale is suggesting that the terms "is provided" and "at the same time" need to be construed, these terms are clear on their face.
said input data being provided to said addressable storage from said first input register at the same time that said output data is provided by said first output register to said system port	Whenever the input data is provided to the addressable storage, the output data must be provided to the system port.	Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent Freescale is suggesting that the terms "being provided" and "at the same time" need to be construed, these terms are clear on their face.

Chan Claim Limitation	Freescale's Constructions	ProMOS's Constructions
said second input data being provided to said addressable storage from said second input register at the same time that said second output data is provided by said second output register to said system port	Whenever the second input data is provided to the RAM, the second output data must be provided to the system port.	Does not need construction. It is not clear which term of this claim element Freescale wishes to construe. To the extent Freescale is suggesting that the terms "being provided" and "at the same time" need to be construed, these terms are clear on their face.
selectively providing input data received from said host port to one of said random access memory, said system port, and said random access memory and said system port	Providing input data received from the host port to: said random access memory and not to said system port under one set of conditions, said system port and not to said random access memory under a second set of conditions, and said random access memory and said system port under a third set of conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's construction of "host port" and "system port" and ProMOS's position on "selectively providing" and "random access memory."
selectively providing	Providing data held in a register depending on certain conditions and never providing data held depending on other conditions.	Does not need construction. To the extent the Court decides to construe the term anyway, it means: providing on a selective basis.
selective provision	Providing data held in a register depending on certain conditions and never providing data held depending on other conditions.	Does not need construction. To the extent the Court decides to construe the term anyway, it means: provision on a selective basis.
selectively providing the first data to one of said random access memory, said system port, and said random access memory and said system port	Providing the first data to: said random access memory and not to said system port under one set of conditions, said system port and not to said random access memory under a second set of conditions, and said random access memory and said system port under a third set of conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's construction of "system port" above, and ProMOS's position on "selectively providing" and "random access memory above.
selectively furnishing first output data to said system port	Furnishing first output data received from the RAM and held in the write back register to said system port depending on certain conditions and never furnishing first output data depending on other conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's construction of "system port" above and ProMOS's position on "selectively furnishing" below.

Chan Claim Limitation	Freescale's Constructions	ProMOS's Constructions
selectively providing second input data to said random access memory	Providing second input data received from the system port and held in the memory update register to said random access memory depending on certain conditions and never providing second input data depending on other conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's position on "selectively writing" below and its position on "random access memory."
selectively furnishing write back data to said system port	Furnishing data received from the RAM and held in the write back register to said system port depending on certain conditions and never furnishing data received from the RAM depending on other conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's construction of "system port" above and ProMOS's position on "selectively furnishing" below.
selectively providing memory write data to one of said random access memory, said system port via said bypass path, and said random access memory and said system port via said bypass path	Providing data buffered in the memory write register from the host port to: -said random access memory and not to said system port under one set of conditions, -said system port via said bypass path and not to said random access memory under a second set of conditions, and -said random access memory and said system port via said bypass path under a third set of conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's construction of "system port" and its position on "selectively providing" and "random access memory."
selectively providing system fetch data to said random access memory	Providing system fetch data received from the system port and held in the memory update register to said random access memory depending on certain conditions and never providing system fetch data depending on other conditions.	Does not need construction. It is not clear which term Freescale wishes to construe. See ProMOS's position on "selectively providing" and "random access memory."
selectively writing	Writing data held in a register depending on certain conditions and never writing data held depending on other conditions.	Does not need construction. To the extent the Court decides to construe the term anyway, it means: writing on a selective basis.
selectively furnishing	Furnishing data held in a register depending on certain conditions and never furnishing data held depending on other conditions.	Does not need construction. To the extent the Court decides to construe anyway, it means: furnishing on a selective basis.

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CERTIFICATE OF SERVICE

I hereby certify that on December 13, 2007, I caused the foregoing to be electronically filed with the Clerk of the Court using CM/ECF which will send electronic notification of such filing to the following:

John G. Day, Esquire
Steven J. Balick, Esquire
ASHBY & GEDDES

Additionally, I hereby certify that true and correct copies of the foregoing were caused to be served on December 13, 2007 upon the following individuals in the manner indicated:

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